CLAIMS:

1. An image decoder comprising:

a code decompression/decoding unit to decode code data produced through compression and encoding of image data;

a power supply state detection unit to detect a current state of a power supply of the image decoder; and

a controller to control the code decompression/decoding unit based on the current state of the power supply so as to reduce power consumption in performing decompression and decoding of the code data.

2. The image decoder according to claim 1, wherein the code decompression/decoding unit includes:

a code discard unit to selectively discard a portion of the code data before the code data are decoded under the control of the controller.

3. The image decoder according to claim 2, wherein the code decompression/decoding unit is operable to decode the code data produced by dividing an image into multiple sub-regions and compressing and encoding the image data in a hierarchical manner for each of the sub-regions.

4. The image decoder according to claim 3, wherein the code decompression/decoding unit is operable to decode the code data produced through compression and encoding of the image data based on the JPEG 2000 algorithm.

5. The image decoder according to claim 2, wherein the controller causes the code discard unit to discard a portion of the code data to decrease a frame rate of the image data in order to reduce the power consumption.

6. The image decoder according to claim 2, wherein the controller causes the code discard unit to discard a portion of the code data to decrease the resolution of the image data in order to reduce the power consumption.

7. The image decoder according to claim 6, wherein the code data is a code stream containing multiple frames, and the controller causes the code discard unit to discard a high-frequency component of each of the frames to decrease the resolution.

8. The image decoder according to claim 2, wherein the controller causes the code discard unit to discard a portion of the code data to decrease an image region to be displayed in order to reduce the power consumption.

9. The image decoder according to claim 8, wherein the code data are produced by dividing an image into multiple sub-regions and performing compression and encoding of the image data of the image for each of the sub-regions, and the code discard unit discards a portion of the sub-regions to allow a center region of the image to be displayed.

10. The image decoder according to claim 2, wherein the controller reduces the frequency of a clock signal used in the code decompression/decoding unit, based on the current state of the power supply, in order to reduce the power consumption.

11. The image decoder according to claim 2, further comprising a variable voltage source to generate a variable voltage from electric power supplied from the power supply to supply the variable voltage to the code decompression/decoding unit, wherein the controller controls the variable voltage source to decrease the variable voltage in order to reduce the power consumption.

12. The image decoder according to claim 2, wherein the code decompression/decoding unit includes an image size reading unit to read an image size from the code data before the decompression/decoding is performed, wherein the controller varies an extent of selective code discard based on the image size.

13. The image decoder according to claim 12, wherein the controller stores two or more tables, each describing parameters for reducing the power consumption in association with the power supply state, and the controller selects an appropriate table based on the image size read by the image size reading unit.

14. The image decoder according to claim 2, further comprising an operation mode setting unit to receive an operation mode selected by a user, wherein when the operation mode setting unit receives the operation mode, the controller varies an extent of selective code discard based on the operation mode selected by the user, regardless of the current state of the power supply.

15. The image decoder according to claim 1, further comprising a communication unit that is in communication with an external apparatus that transmits the code data to the image decoder, wherein the controller determines a standard for selectively discarding a portion of the code data based on the current state of the power supply, and instructs the external apparatus to discard a portion of the code data before the code data are transmitted to the image decoder.

16. An image coder comprising:

an image compression/encoding unit to perform compression and encoding of an image;

a power supply state detector to detect a current state of a power supply of the image coder; and

a first mode setting unit to select a processing mode for compression/encoding

rate control in accordance with the current state of the power supply.

17. The image coder according to claim 16, wherein the first mode setting unit selects a Lagragian rate control mode when the current state of the power supply is above a reference state and selects a plain rate control mode when the current state of the power supply is at or below the reference state.

18. The image coder according to claim 17, wherein when the plain rate control mode is selected, the image compression/encoding unit discards a portion of a code stream in a prescribed manner with reference to a target code amount.

19. The image coder according to claim 18, wherein the image compression/encoding unit has a discard order table that describes code discard patterns, and discards the portion of the code stream with reference to the discard order table and the target code amount.

20. An image coder comprising:

an image compression/encoding unit to divide an image into a plurality of tiles through a tiling process and perform compression and encoding of the image in a hierarchical manner for each of the tiles;

a power supply state detector to detect a current state of a power supply of the image coder; and

a first mode setting unit to select a tiling processing mode in accordance with the current state of the power supply.

21. The image coder according to claim 20, wherein the first mode setting unit selects an overlap tiling mode when the current state of the power supply is above a reference state and selects a non-overlap tiling processing mode when the current state of the power supply is at or below the reference state.

22. An image coder comprising:

an image compression/encoding unit to perform compression and encoding of an image using wavelet transform for frequency transform;

a power supply state detector to detect a current state of a power supply of the image coder; and

a first mode setting unit to select a processing mode of wavelet transform in accordance with the current state of the power supply.

23. The image coder according to claim 22, further comprising a wavelet filter, wherein the first mode setting unit selects the number of taps of the wavelet filter in accordance with the current state of the power supply.

24. The image coder according to claim 23, wherein the first mode setting unit selects a 9-tap/7-tap filter when the current state of the power supply is above a reference state, and it selects a 5-tap/3-tap filter when the current state of the power supply is at or below the reference state.

25. The image coder according to claim 22, wherein the first mode setting unit selects a hierarchical level of wavelet transform in accordance with the current state of the power supply.

26. The image coder according to claim 25, wherein the first mode setting unit selects a 5-level wavelet transform when the current state of the power supply is above a reference state and selects a 3-level wavelet transform when the current state of the power supply is at or below the reference state.

27. The image coder according to claim 16, 20, or 22, further comprising a second mode setting unit to accept a user's selection of an operation mode and to

select a processing mode of the image compression/encoding unit, regardless of the selection of the mode by the first mode setting unit.

28. The image coder according to claim 27, further comprising:

a variable voltage source to supply a variable voltage to the image compression/encoding unit, the variable voltage being changed in accordance with the operation mode selected by the second mode setting unit.

29. The image coder according to claim 27, further comprising:

a clock generator to generate and supply a clock signal to the image compression/encoding unit, the frequency of the clock signal being changed in accordance with the operation mode selected by the second mode setting unit.

30. The image coder according to claim 16, 20, or 22, further comprising:

a variable voltage source to supply a variable voltage to the image compression/encoding unit, the variable voltage being changed in accordance with the processing mode selected by the first mode setting unit.

31. The image coder according to claim 16, 20, or 22, further comprising:

a clock generator to generate and supply a clock signal to the image compression/encoding unit, the frequency of the clock signal being changed in accordance with the processing mode selected by the first mode setting unit.